



General Features

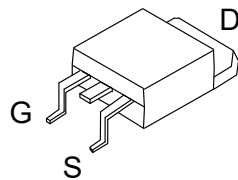
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

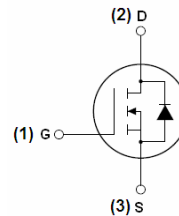
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Product Summary

BVDSS	60	V
$R_{DS(on)}$, Typ. @ $V_{GS}=10V$	23	$m\Omega$
ID	30	A



TO-252



Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous ($T_C=100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	14	A
Pulsed Drain Current	I_{DM}	120	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.3	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	82	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.3	$^\circ\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

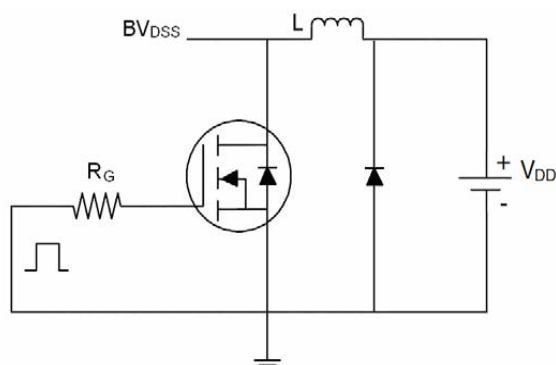
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	23	29	mΩ
		V _{GS} =4.5V, I _D =10A		29	40	
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =10A	11	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	1932	-	PF
Output Capacitance	C _{Oss}		-	135	-	PF
Reverse Transfer Capacitance	C _{rss}		-	39.5	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =3Ω V _{GS} =10V, R _G =3Ω	-	7	-	nS
Turn-on Rise Time	t _r		-	20	-	nS
Turn-Off Delay Time	t _{d(off)}		-	16	-	nS
Turn-Off Fall Time	t _f		-	23	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =10A, V _{GS} =10V	-	25		nC
Gate-Source Charge	Q _{gs}		-	4.5		nC
Gate-Drain Charge	Q _{gd}		-	6.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =10A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	30	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =10A di/dt = 100A/μs ^(Note3)	-	29	-	nS
Reverse Recovery Charge	Q _{rr}		-	49	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

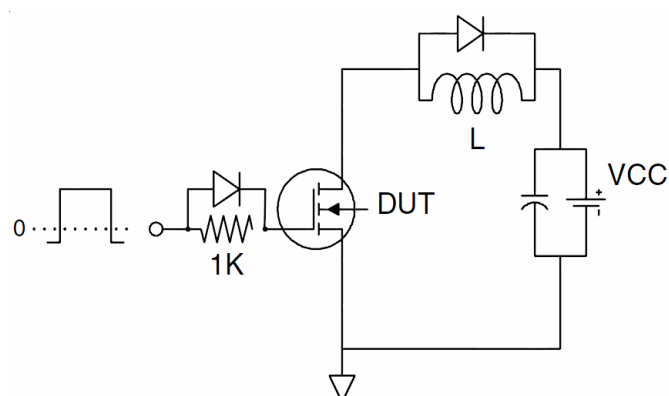
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

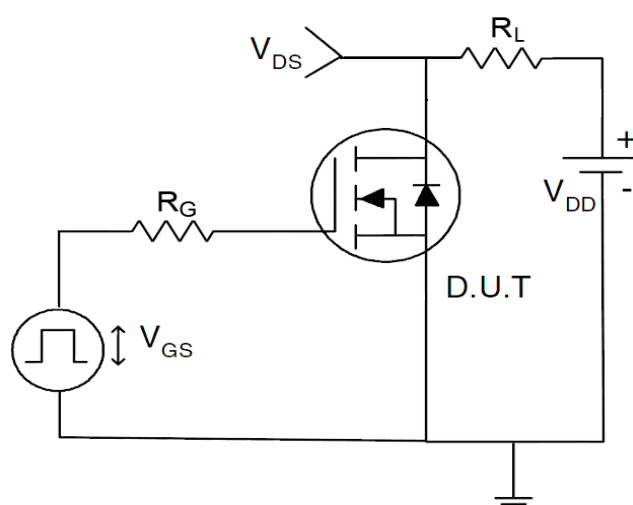
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

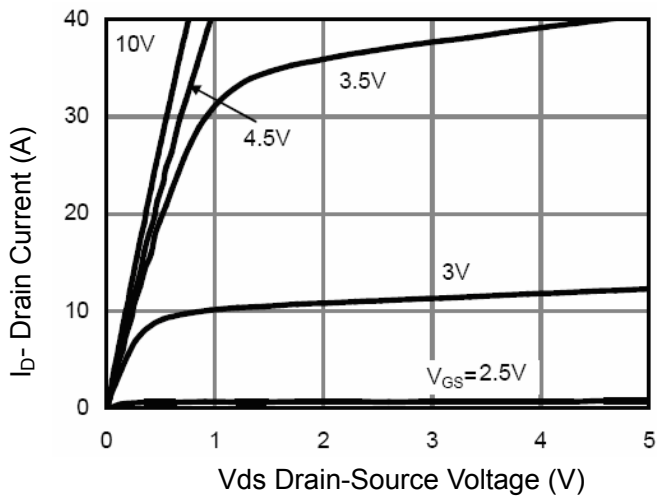


Figure 1 Output Characteristics

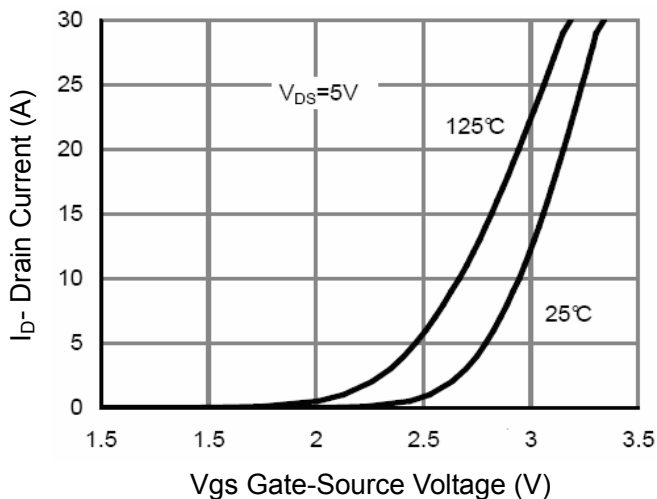


Figure 2 Transfer Characteristics

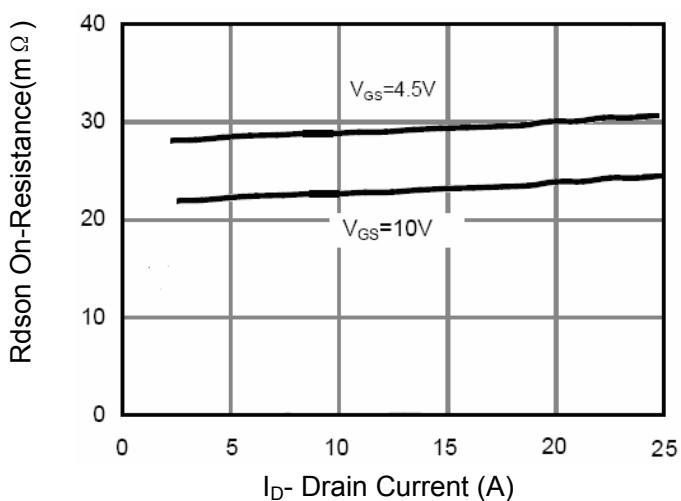


Figure 3 $R_{DS(on)}$ - Drain Current

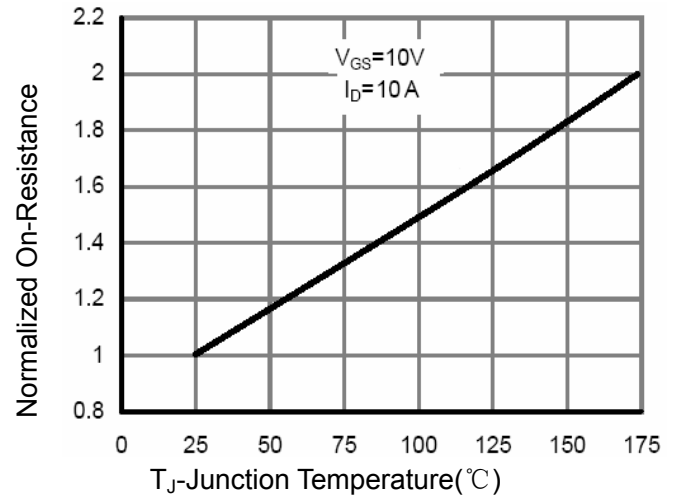


Figure 4 $R_{DS(on)}$ -Junction Temperature

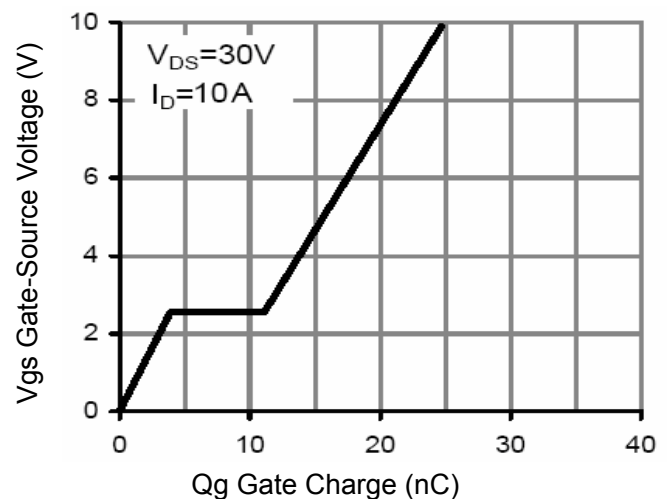


Figure 5 Gate Charge

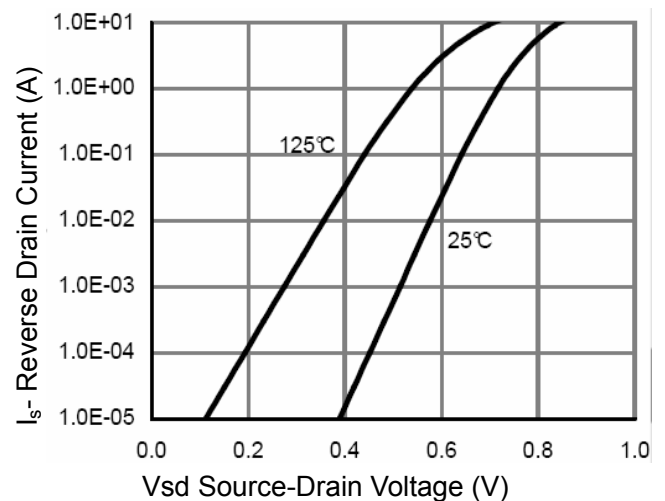


Figure 6 Source- Drain Diode Forward

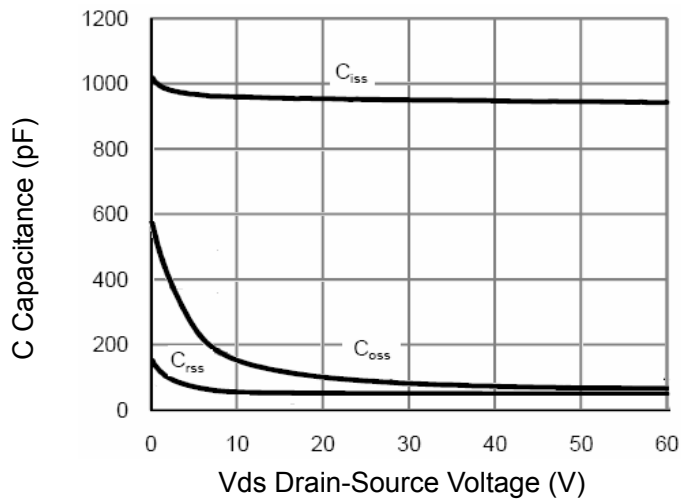


Figure 7 Capacitance vs Vds

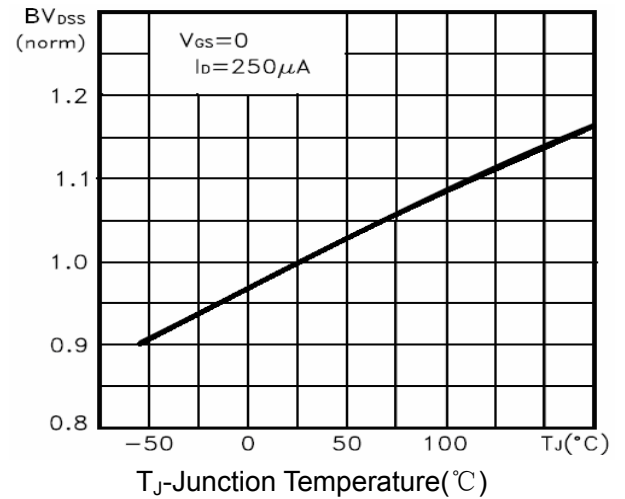


Figure 9 BV_{DSS} vs Junction Temperature

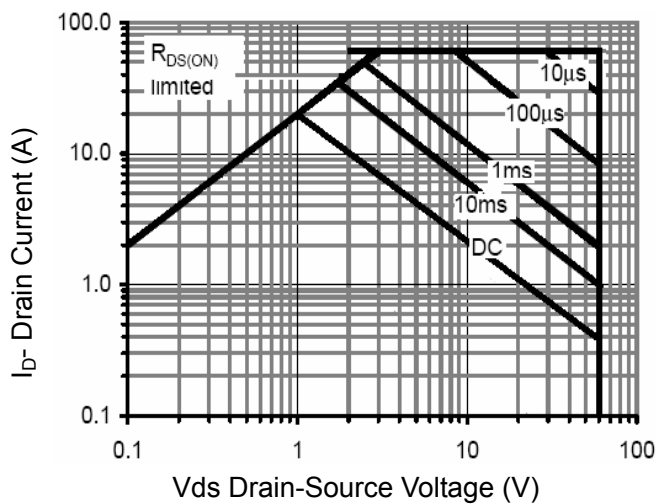


Figure 8 Safe Operation Area

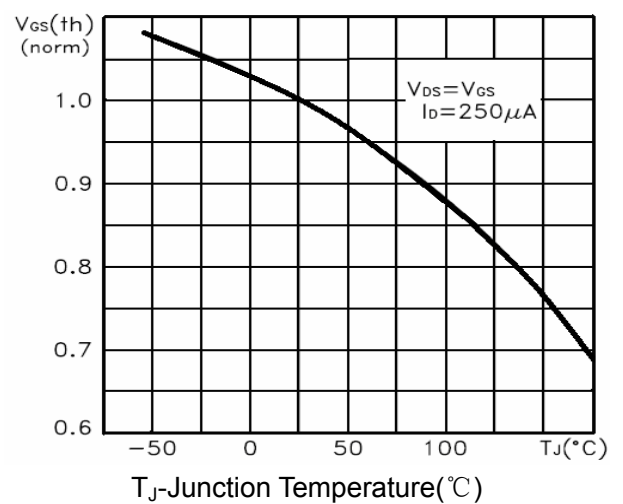


Figure 10 $V_{GS(th)}$ vs Junction Temperature

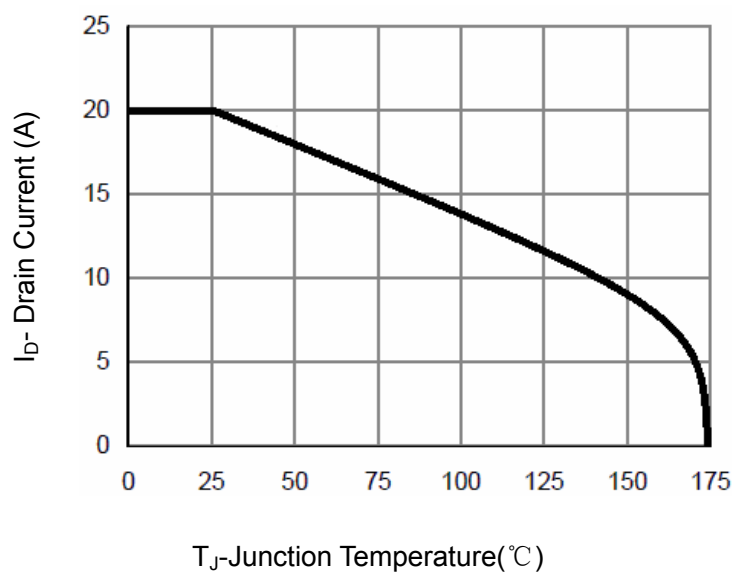


Figure 11 Current De-rating

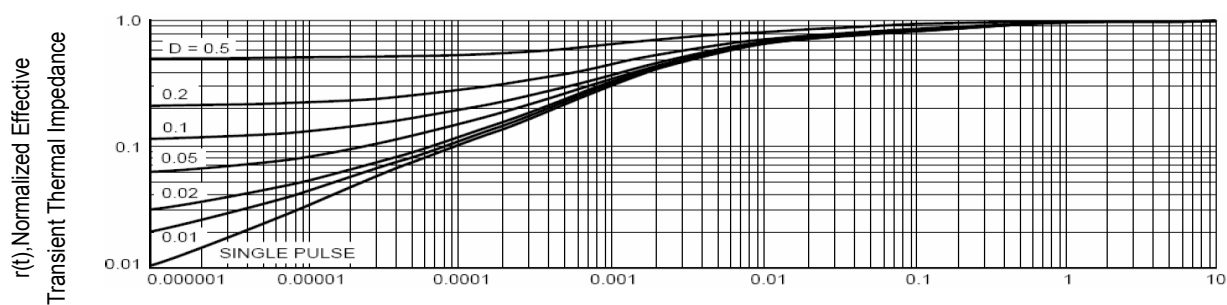
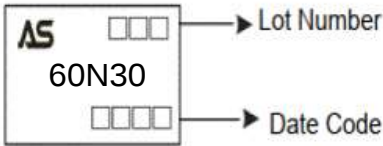
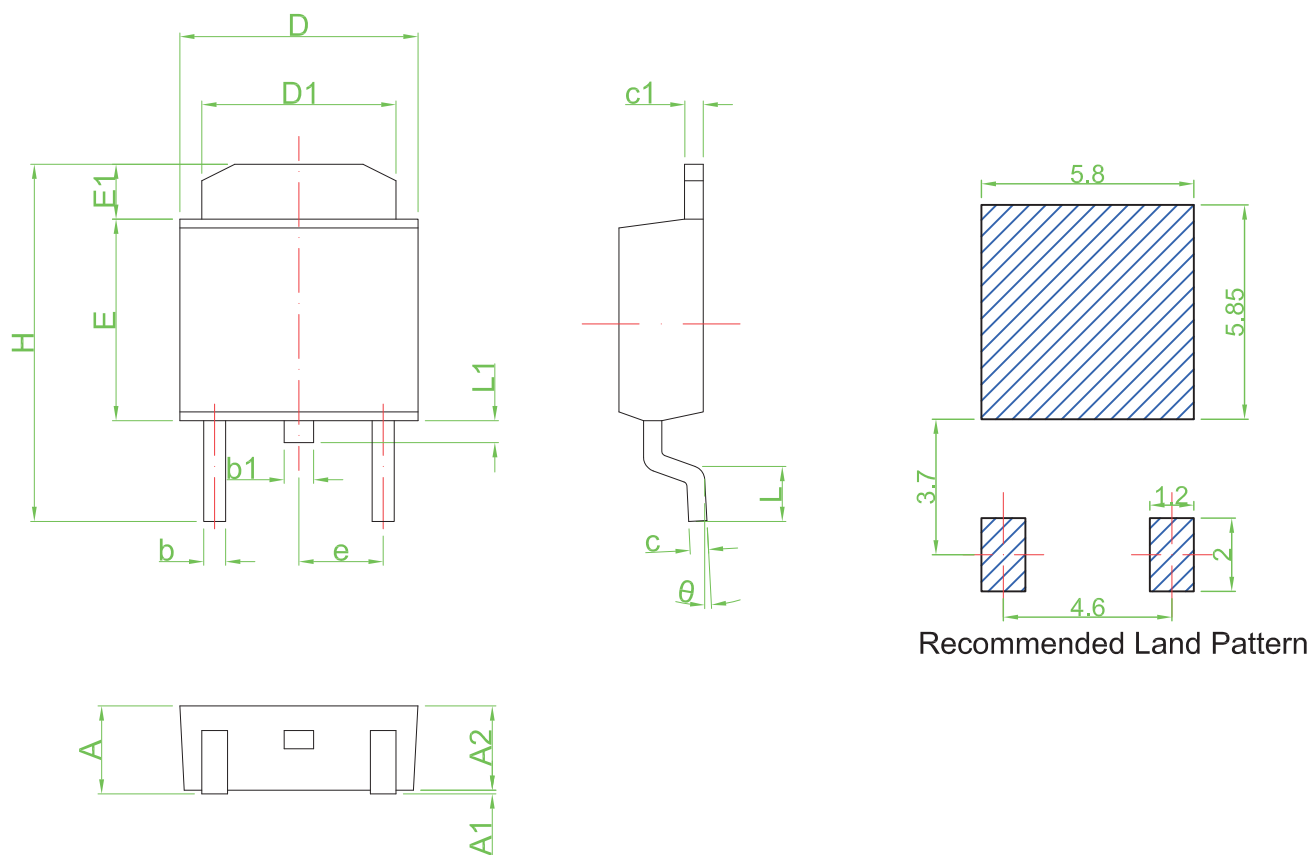


Figure 12 Normalized Maximum Transient Thermal Impedance

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM60N30KQ-R	60N30	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 The diagram shows a rectangular marking area on a TO-252 package. It contains the ASDsemi logo (AS) in the top left, the part number 60N30 in the center, and two sets of four empty boxes (□□□□) for Lot Number and Date Code. Arrows point from the text 'Lot Number' and 'Date Code' to their respective box sets.



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.25	2.65	0.089	0.104
A1	0.00	0.15	0.000	0.006
A2	2.20	2.40	0.087	0.094
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.46	0.66	0.018	0.026
c1	0.46	0.66	0.018	0.026
D	6.30	6.70	0.248	0.264
D1	5.20	5.40	0.205	0.213
E	5.30	5.70	0.209	0.224
E1	1.40	1.60	0.055	0.063
H	9.40	9.90	0.370	0.390
e	2.30 TYP		0.09 TYP	
L	1.40	1.77	0.055	0.070
L1	0.50	0.70	0.020	0.028
θ	0°	8°	0°	8°

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